PATENT SPECIFICATION (11) 1 279 167

DRAWINGS ATTACHED

1 279 167

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(54) METHOD OF MANUFACTURING BEAM LEAD INTEGRATED CIRCUITS

(71) We, ITT INDUSTRIES, INC., a Corporation organised and existing under the laws of the State of Delaware, United States of America, of 320 Park Avenue, New York 22, State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the fabrication of integrated circuit devices which have improved a.c. and d.c. electrical isolation between discrete components of the integrated circuit.

One method of forming beam lead integrated circuit devices has been to form various discrete components within a wafer and provide the appropriate interconnection lead pattern on a surface thereof. The opposite side of the wafer is then masked to expose portions of the wafer surrounding each discrete component. A suitable etchant is then applied to the masked surface so as to remove a portion of the wafer material which surrounds each discrete component. After this occurs the complete integrated circuit devices on the wafer separate from one another and each device contains isolated discrete components which are held together by the beam leads.

It is thus seen that using this approach the individual components become very hard to handle and the main support for each component must be supplied by the interconnection leads. Therefore, these leads must be sufficiently thick in order to be able to support the circuit, such thickness necessarily being greater than 20 microns. Due to the required thickness of these beam leads, aluminium interconnection leads cannot be used because it is too difficult and impractical to obtain interconnection aluminium beam leads of required thickness. Therefore, a more expensive combination such as platinum, titanium and gold must be used. The platinum first contacts the surface. The titanium would then be used as an intermediate layer so that the final layer of gold would properly adhere to the combination.

Furthermore, since these wafers must be very thin, approximately 1 to 2 mils, the devices cannot dissipate much heat except through the beam lead sleeves thereby reducing the suitability for these devices in various applications requiring a designated minimum power dissipation.

It is an object of this invention to provide an improved method of fabricating beam lead integrated circuit devices.

It is a further object to provide a beam lead integrated circuit component having improved heat dissipation, and a.c. and d.c. electrical isolation characteristics.

According to the present invention there is provided a method of manufacturing an integrated circuit semiconductor device comprising the steps of forming a composite body including a semiconductor wafer, an intermediate glass layer and a heat dissipating substrate of the same thermal coefficient of expansion as the wafer, the wafer containing discrete electrical components within a surface thereof, which surface froms a surface of the composite body, forming lead connections between designated discrete electrical components, and removing wafer material from the wafer surface down to the glass layer around the discrete electrical components and beneath the lead connections, so as to electrically isolate the discrete components from one another except for the connections provided by the lead connections.

Embodiments of the invention will now be described with reference to the accompanying drawings, in which

Figs. 1 to 6 show a portion of the wafer

and the sequence of steps depicting the invention therein;

Fig. 8 shows a top view of a portion of the wafer after the final step in the process; and

Fig. 7 shows a cross-section of Fig. 8 taken along line X-X'.

A portion of the composite body shown in Fig. 4 may be formed by a number of alternate sequences of operations. One such sequence will now be described. We can start with a cylindrical shaped substrate having a one-inch diameter and being from 10 to 12 mils thick. The resistivity of the substrate material is non-critical, and may be typically in a range of between .1 to 100 ohm-cm. It should have good thermal characteristics so that the heat dissipation of the final device would be better than the device described in the background of the invention. The substrate will also provide greater ease in handling for final devices so as to facilitate the final packaging and assembling thereof. The substrate material should have the same thermal coefficient of expansion as the wafer used in order that the composite body would have the minimum stress introduced therein during wide temperature excursions. For integrated circuits having good high frequency and thermal characteristics, silicon material is most often used and in these cases substrate 1 in Fig. 1 can be composed of silicon. Although substrate 1 has been described as being composed of silicon semiconductor material, other suitable materials such as gallium arsenide or germanium could be used for certain devices.

Fig. 2 shows the composite sandwich of substrate 1, interposed intermediate glass layer 2, and wafer 3. Wafer 3 in this example is also composed of silicon of one inch in diameter and 10 to 12 mils in thickness. Wafer 3 likewise can be any required resistivity depending upon the design considerations for the final integrated circuit device. The resistivity range of .1 to 100 ohm-cm for wafer 3 can be used. Also, other materials such as germanium or gallium arsenide could be substituted for silicon in wafer 3. Generally, the intermediate glass layer 2 which is used can be of any suitable material which will electrically isolate the substrate and the wafer, have the same coefficient of expansion as the substrate and wafer and have a soft point temperature higher than those temperatures encountered during the diffusion of impurities into the wafer. There are available glasses, such as type 1715 glass made by Corning Glass, which has a coefficient of expansion similar to silicon and a soft point of about 1100°C. This material would be suitable when first forming a composite body as shown in Fig. 4. The aluminosilicate glass generally comes in a powder frit and can be mixed with alcohol to form a suspension. This suspension can then be applied to the surface of substrate 1 and used in conjunction with a centrifuge to obtain a suitable suspension of the alumino-silicate glass of approximately 1 mil in thickness on a surface of the substrate. The wafer 3 is then placed over the suspension and the sandwich formed therein can be placed between carbon susceptors affixed to a hydraulic press. R.F. coils can be coupled to the carbon susceptors so as to provide a source of heat by radio frequency induction to the carbon susceptors. The package can then be heated to approximately 1200°C and at the same time have a pressure of approximately 1200 lbs. per square inch applied thereto. After the temperature of 1200°C is reached, the package is cooled to room temperature while the pressure of 1200 lbs. per square inch is maintained, after which time the pressure is released. This ensures that the composite body shown in Fig. 2 will be securely bonded together.

It is now necessary to reduce the thickness of wafer 3 to approximately one-half a mil as shown in Fig. 3 as indicated by the reduced thickness of wafer 3*a*. It is important that the opposite surfaces of reduced wafer 3 be reasonably parallel. The most convenient way of carrying out this reduction of the thickness of wafer 3 is by placing the body in a Hoffmann Planetary lapper so that the surface of the wafer is reduced in a reasonably parallel fashion. If a two-face lapping process was applied to the composite body, then the original substrate in all probability should be between 20 and 24 mils in thickness so that both wafer 3*a* and substrate 1 would have been reduced in thickness by about the same amount. An alternate way of reducing wafer 3*a* would be to chemically thin wafer 3 to approximately 1 mil by using any known etching solution such as one containing hydrofluoric acid, nitric acid and acetic acid in suitable proportions. The wafer would then be reduced to its final size of about one-half mil by polishing its surface with a silicon dioxide slurry solution.

Electrical components 4 shown in Fig. 4 can then be formed within the surface of water 3*a*. Any number of active or passive components can be formed therein using standard photolithographic masking, diffusion and deposition techniques well known in the art and described in any number of textbooks such as "Integrated Circuit Design Principles and Fabrications" by Warner and Fordemwalt, 1965. It is of course possible to form the composite body shown in Fig. 4 in alternate fashions such as by applying a low temperature glaze to substrate 1 and placing a thin wafer 3*a*

having the required discrete components already formed therein, on the glazed surface. In this example, the glaze should probably have a soft point temperature appreciably lower than the temperature required during the diffusion steps when forming the original components so as not to effect the electrical characteristics of the previously formed components.

The desired interconnection leads for the integrated circuit device can now be formed. The surface of wafer 3*a* is first suitably masked with a passivation layer 5 as shown in Fig. 5 leaving terminal contact areas to the individual components exposed through suitable holes in the masking layer. The passivation layer should preferably be an oxide of silicon such as silicon dioxide. This layer 5 can be formed by standard evaporation techniques known in the art. Other suitable masking materials, such as silicon nitride, can also be used wherein silicon nitride can be deposited using standard R.F. glow discharge techniques as described in United Kingdom Patent Specification No. 1 104 935. The passivation layer should first be deposited to a thickness of 1 micron or less so as to completely cover all of surface 3*a*. Using standard well known photolithographic techniques well known in the art, holes can be selectively etched in the passivation layer 5 to expose desired terminals of discrete components formed within the wafer surface. A common etch which could be used in the removal of silicon dioxide is diluted HF plus ammonium fluoride having a volume ratio of 4 : 1 NH_4F : HF. A suitable metallization layer is then evaporated over the entire masked surface and exposed component terminals. A suitable metal would be aluminium which can be deposited to approximately 4 to 10 microns in thickness by any known technique such as electron beam evaporation, filament evaporation or glow discharge. Again, using standard photolithographic techniques herein mentioned above, the desired interconnecting lead pattern is finally formed by selectively etching unwanted aluminium which is exposed through holes in the developed resist pattern. A suitable aluminium etchant could be a solution of sodium hydroxide. The leads of this final interconnection lead pattern should be less than approximately 1 mil wide. Of course, aluminium has been given as an example because it is economical to use. However, other suitable materials can be used for forming an interconnection pattern. One such example is the more expensive combination sandwich layer of platinum, titanium and gold wherein the platinum is deposited over the silicon surface, the titanium being deposited over the platinum layer and gold being deposited over the titanium layer.

After the desired interconnection lead pattern is formed, as shown in Fig. 6 by leads 6, we begin to remove the silicon material completely around each discrete component from the wafer surface to glass layer 2 and underneath lead 6 so as to completely d.c. and a.c. electrically isolate each individual portion 3*b* of the wafer 3*a* from the other by the intervening air gap 7 as shown in Figs. 7 and 8. This is accomplished by first removing portions of the passivating layer 5 to expose the overlying wafer surface. The portions of layer 5 to be removed, may extend in a direction surrounding each individual component and abut each lead 6. This is accomplished again using standard photolithographic techniques to expose only those portions of the layer which are to be removed and then immersing the body in a suitable buffered etchant, such as the 4 : 1 NH_4F : HF referred to above. After the wafer surface has been exposed in the above described manner, the composite body may then be immersed in a known suitable etchant, such as HF plus nitric acid plus acetic acid suitable proportioned and/or diluted. One such etchant is commonly known as CP6.

As can be seen from Figs. 7 and 8 the CP6 will preferentially remove the exposed silicon to the full depth of wafer 3*a* until it is stopped by glass layer 2 which is not affected by the CP6. Since the wafer thickness is approximately one-half mil and the width of each lead is approximately 1 mil, as the etchant removes the one-half mil thick silicon of wafer 3*a*, one-half mil of silicon material under each side of lead 6 is undercut at the same rate that the silicon is being removed from exposed areas. The etchant does not have enough time therefore to penterate too far underneath the passivating layer 5 and therefore does not actually attack or effect the portions 3*b* of the wafer 3*a*. After this process is completed, the substrate may be carrying a number of separate independent integrated circuit components. Applying ordinary scribing techniques well known in the art, the substrate can be subdivided and separate integrated circuit devices can be formed and packaged separately, for example in a TO-50 package.

WHAT WE CLAIM IS:—

1. A method of manufacturing an integrated circuit semiconductor device comprising the steps of:

forming a composite body including a semiconductor wafer, an intermediate glass layer and a heat dissipating substrate of the same thermal coefficient of expansion as the wafer, the wafer containing discrete electrical components within a surface thereof, which surface forms a

surface of the composite body;

forming lead connections between designated discrete electrical components; and

removing wafer material from the wafer surface down to the glass layer around the discrete electrical components and beneath the lead connections, so as to electrically isolate the discrete components from one another except for the connections provided by the lead connections.

2. A method of manufacturing a semiconductor device as claimed in claim 1, wherein the composite body is formed by the further steps of:

depositing a glass on a silicon substrate;

placing a silicon wafer over the glass to form a sandwich;

placing the sandwich between carbon susceptors affixed to a hydraulic press;

heating the sandwich to approximately 1200°C under approximately 1200 lbs. per square inch of pressure;

cooling the sandwich to room temperature while maintaining the pressure; and

releasing the pressure.

3. A method of manufacturing a semiconductor device as claimed in claim 2, wherein the glass is deposited on said substrate by mixing glass frits in an alcohol suspension, and applying the mixture to the substrate.

4. A method of manufacturing a semiconductor device as claimed in claim 2 or 3, wherein heat is supplied to the carbon susceptors by radio frequency induction.

5. A method of manufacturing a semiconductor device as claimed in any one of claims 2-4, wherein after the step of releasing the pressure, the electrical components are formed within the surface of the wafer using photolithographic masking, diffusion and deposition techniques.

6. A method of manufacturing a semiconductor device as claimed in claim 1, wherein the lead connections are formed by the further steps of:

coating the wafer surface with a passivating mask having holes therein to expose terminals of the discrete components;

depositing a metal layer over the mask and exposed terminals; and

selectively removing the metal layer to form the interconnecting leads between the designated discrete components.

7. A method of manufacturing a semiconductor device as claimed in claim 6, wherein the mask is an oxide of silicon having a thickness of less than approximately 1μ.

8. A method of manufacturing a semiconductor device as claimed in claim 6, wherein the mask is a nitride of silicon having a thickness of less than approximately 1μ.

9. A method of manufacturing a semiconductor device as claimed in claim 6, wherein the metal layer consists of aluminium of at least 4μ in thickness.

10. A method of manufacturing a semiconductor device as claimed in claim 6, wherein the metal layer comprises a layer of platinum contiguous with the wafer, a layer of titanium contiguous with the platinum layer, and a layer of gold contiguous with the titanium layer.

11. A method of manufacturing a semiconductor device as claimed in claim 9, wherein the aluminium is selectively removed by photolithographically forming the desired interconnection pattern over the aluminium leaving areas of exposed aluminium, and immersing the body in an aluminium etchant to remove the exposed aluminium while leaving the desired interconnection pattern on the wafer.

12. A method of manufacturing a semiconductor device as claimed in claim 6, wherein the wafer material is removed by the further steps of:

removing portions of the mask to expose the underlying wafer surface, the portions being adjacent the overlying part of the leads between each component, and extending in a direction surrounding each discrete component; and

immersing the body in an etchant which selectively removes only wafer material in a preferential manner so as to undercut the leads and completely isolate each discrete component.

13. A method of manufacturing an integrated circuit semiconductor device substantially as herein described with reference to the accompanying drawings.

14. An integrated circuit semiconductor device made by a method as claimed in any one of the preceding claims.

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For the Applicant.

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2 SHEETS

COMPLETE SPECIFICATION

SHEET 1

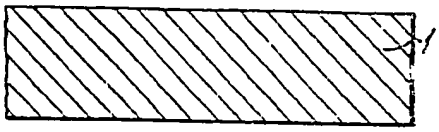

Fig.1.

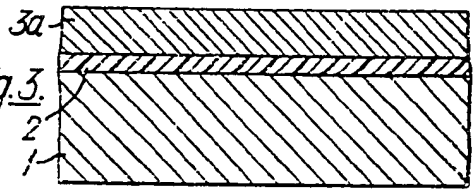

Fig.3.

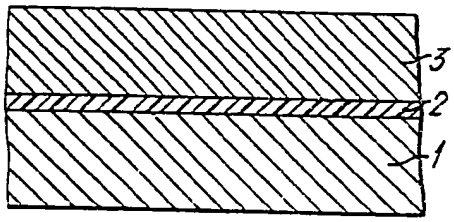

Fig.2.

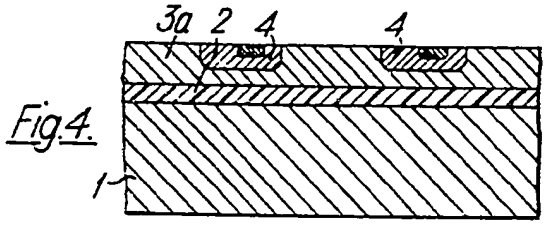

Fig.4.

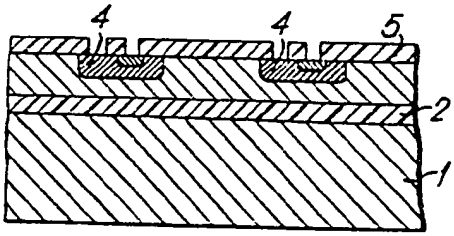

Fig.5.

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COMPLETE SPECIFICATION

This drawing is a reproduction of the Original on a reduced scale.

SHEET 2

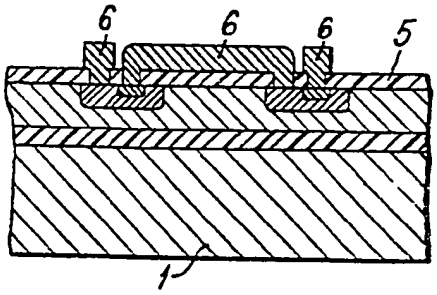

Fig. 6.

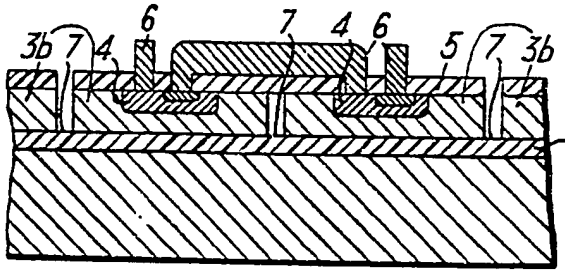

Fig. 7.

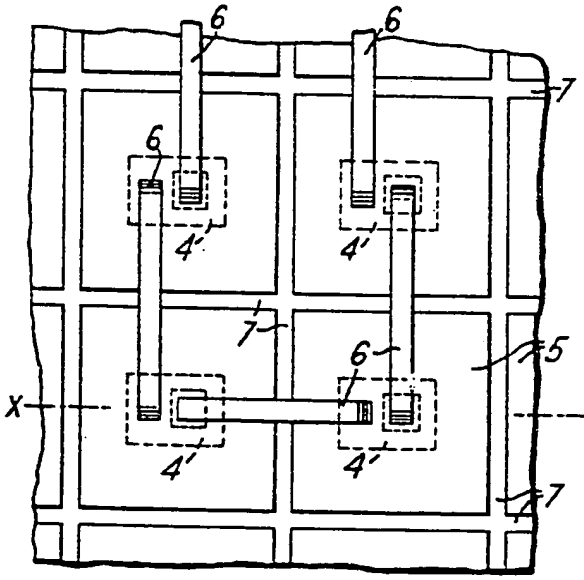

Fig. 8